WHAT IS CLAIMED IS:

1. An apparatus for managing operations in a processor, said apparatus comprising:

a plurality of addressable registers, each of said registers partitioned into plurality of data entry fields;

a first comparison circuit, said first comparison circuit operable to scan and compare a value in a set of said data entry fields to a predetermined input value;

a second comparison circuit, said second comparison circuit operable to compare a first register address corresponding to a comparison match of said first comparison circuit to a second register address; and

a dispatch circuit operable to dispatch data of a second data entry field of a second register corresponding to said second register address to an operation unit in response to a decode of data in a third data entry field of said second register and a comparison match of said second comparison circuit.

2. The apparatus of claim 1, wherein said operations are Load and Store operations within said processor.

3. The apparatus of claim 1, wherein said predetermined input value is a real address requesting particular data corresponding to one of a Load and a Store operation.

4. The apparatus of claim 1, wherein said first scan comparison circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison circuits operable concurrently in parallel.

5. The apparatus of claim 1, wherein said operation unit comprises an Instruction Management Unit (IMU).

6. The apparatus of claim 1, wherein said operation unit comprises a Storage Management Unit (SMU) said SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB).

7. The apparatus of claim 1, wherein one of said data entry fields is a Valid bit field, said Valid bit field indicating whether other data entry fields are valid.

8. The apparatus of claim 1, wherein one of said data entry fields is an Instruction Identification (ID) field corresponding to a particular Load and Store operation.

9. The apparatus of claim 1, wherein one of said data entry fields is an Instruction status field corresponding to a status of one of said Load and Store operations.

10. The apparatus of claim 1, wherein one of said data entry fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load operation if said Load/Store bit has a first logic state and corresponding to a Store operation if said Load/Store bit has a second logic state.

11. The apparatus of claim of claim 1, wherein one of said data entry fields comprises Real Address field, said Real Address field corresponding to a particular Real Address of memory data.

12. The apparatus of claim 1, wherein one of said data entry fields is a Quadword field, said Quadword field comprising multiple bytes of data.

13. The apparatus of claim 1, wherein one of said data entry fields is an Operand Mask field, said Operand Mask field defining selected bytes of data within a selected one of said data entry fields.

14. The apparatus of claim 1, wherein said operation unit is a pipeline execution unit operating concurrently on a plurality of said data entry fields.

15. The apparatus of claim 1, wherein said addressable registers are addressed using a plurality of address pointers.

16. The apparatus of claim 1 wherein said addressable registers are configured as said Storage Reference Buffer (SRB).

17. The apparatus of claim 15, wherein one of said address pointers is a third pointer, said third pointer, said third pointer pointing to one of said addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation.

18. The apparatus of claim 15, wherein said address pointers comprise a fourth and a fifth pointer, said fourth and fifth pointers defining a window of register addresses from which a Load operation may be satisfied without having to access other memory storage.

19. The apparatus of claim 15, wherein said second register address is selected from registers addresses which fall within a window of register addresses, said window of addresses defined by said address pointers.

20. The apparatus of claim 15, wherein one of said address pointers is a first pointer, said first pointer pointing to an IN register address of a first available register into which data may be added.

21. The apparatus of claim 15, wherein one of said address pointers is a second pointer, said second pointer pointing to an OUT register address of a first available register from which register data may be retired.

22. The apparatus of claim 16, wherein said data entry fields, added to said SRB after a mis-predicted branch instruction occurs in said processor, are retired and said first pointer is indexed to first register address of a register with added register data entry bits which were added immediately prior to said mis-predicted branch instruction.

23. The apparatus of claim 19, wherein said window of register addresses defines active Load and Store operations.

24. The apparatus of claim 20, wherein said first pointer is indexed by one when said register data has been added, said first pointer having a minimum and a maximum value wherein a decrement down from a minimum value results in said maximum value and an increment up from said maximum value results in said minimum value.

25. The apparatus of claim 21, wherein said second pointer is indexed by one when register entry bits have been deleted, said second pointer having a minimum and a maximum value wherein a decrement down from said minimum value results in said maximum value and an increment up from said maximum value results in said minimum value.

26. A data processing system, comprising:

a central processing unit (CPU);

random access memory (RAM);

read only memory (ROM);

an I/O adapter; and

a bus system coupling devices internal to said CPU, said CPU comprising an apparatus for managing operations within a processor of said CPU, said apparatus comprising:

a plurality of addressable registers, each of said addressable registers partitioned into plurality of data entry fields;

a first comparison circuit, said first comparison circuit operable to scan and compare a predetermined input value to a value from a first data entry field selected from each of said addressable registers;

a second comparison circuit, said second comparison circuit operable to compare a first register address corresponding to a comparison match of said first comparison circuit to a second register address; and

a dispatch circuit operable to dispatch data in a second data entry field of a second register to an operation unit, said second register corresponding to said second register address in response to a decode

of data in a third data entry field of said second register and a comparison match of said second comparison circuit.

27. The data processing system of claim 26, wherein said operations are Load and Store operations within said processor.

28. The data processing system of claim 26, wherein said predetermined input value is a real address requesting particular data corresponding to one of a Load and a Store operation.

29. The data processing system of claim 26, wherein said first scan comparison circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison circuits operable concurrently in parallel.

30. The data processing system of claim 26, wherein said operation unit comprises an Instruction Management Unit (IMU).

31. The data processing system of claim 26, wherein said operation unit comprises a Storage Management Unit (SMU) said SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB).

32. The data processing system of claim 26, wherein one of said data entry fields is a Valid bit field, said Valid bit field indicating whether other data entry fields are valid.

33. The data processing system of claim 26, wherein one of said data entry fields is an Instruction Identification (ID) field corresponding to a particular Load and Store operation.

34. The data processing system of claim 26, wherein one of said data entry fields is an Instruction status field corresponding to a status of one of said Load and Store operations.

35. The data processing system of claim 26, wherein one of said data entry fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load operation if said Load/Store bit has a first logic state and corresponding to a Store operation if said Load/Store bit has a second logic state.

36. The data processing system of claim of claim 26, wherein one of said data entry fields comprises Real Address field, said Real Address field corresponding to a particular Real Address of memory data.

37. The data processing system of claim 26, wherein one of said data entry fields is a Quadword field, said Quadword field comprising multiple bytes of data.

38. The data processing system of claim 26, wherein one of said data entry fields is an Operand Mask field, said Operand Mask field defining selected bytes of data within a selected one of said data entry fields.

39. The data processing system of claim 26, wherein said operation unit is a pipeline execution unit operating concurrently on a plurality of said data entry fields.

40. The data processing system of claim 26, wherein said addressable registers are addressed using a plurality of address pointers.

41. The data processing system of claim 26 wherein said addressable registers are configured as said Storage Reference Buffer (SRB).

42. The data processing system of claim 40, wherein one of said address pointers is a third pointer, said third pointer, said third pointer pointing to one of said addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation.

43. The data processing system of claim 40, wherein said address pointers comprise a fourth and a fifth pointer, said fourth and fifth pointers defining a window of register addresses from which a Load operation may be satisfied without having to access other memory storage.

44. The data processing system of claim 40, wherein said second register address is selected from registers addresses which fall within a window of register addresses, said window of addresses defined by said address pointers.

45. The data processing system of claim 40, wherein one of said address pointers is a first pointer, said first pointer pointing to an IN register address of a first available register into which data may be added.

46. The data processing system of claim 40, wherein one of said address pointers is a second pointer, said second pointer pointing to an OUT register address of a first available register from which register data may be retired.

47. The data processing system of claim 41, wherein said data entry fields, added to said SRB after a mis-predicted branch instruction occurs in said processor, are retired and said first pointer is indexed to first register address of a register with added register data entry bits which were added immediately prior to said mis-predicted branch instruction.

48. The data processing system of claim 44, wherein said window of register addresses defines active Load and Store operations.

49. The data processing system of claim 45, wherein said first pointer is indexed by one when said register data has been added, said first pointer having a minimum and a maximum value wherein a decrement down from a minimum value results in said maximum value and an increment up from said maximum value results in said minimum value.

50. The data processing system of claim 46, wherein said second pointer is indexed by one when register entry bits have been deleted, said second pointer having a minimum and a maximum value wherein a decrement down from said minimum value results in said maximum value and an increment up from said maximum value results in said minimum value.

51. A method for a Load operation in a Load and Store operation unit comprising the steps of:

issuing concurrently a fetch instruction requesting a real address to a data cache and a Storage Reference Buffer (SRB), said real address corresponding to an address of multiple bytes of data;

checking said SRB for said real address;

receiving said multiple bytes of data from said SRB if said real address is available;

retrieving said multiple bytes of data first from said SRB if said real address is available and second from said data cache if said real address is not available in said SRB; and

updating a corresponding SRB register with said multiple bytes of data.

52. A method for a Store operation in a Load and Store operation unit comprising the steps of:

issuing a real address generation instruction;

looking up said real address in a table lookup buffer;

sending said real address to a miss resolution processor if said real address is not in said table lookup buffer, said miss resolution processor determining a translated real address;

sending said real address from one of said miss resolution processor and said table lookup buffer to a Storage Reference Buffer (SRB); and

updating corresponding data entry fields in said SRB.

53. A method for a Store operation in a Load and Store operation unit comprising the steps of:

issuing an address generation instruction by a first instruction unit, said address generation instruction generating a real address in memory;

updating said real address in a real address field of a register in a Storage Reference Buffer;

sending concurrently, a request for a multiple byte word with said real address to said Storage Reference Buffer and a data cache;

receiving said multiple byte word from one of said Storage Reference Buffer and said data cache;

updating said multiple byte word from said data cache with an operand mask;

receiving from said first instruction unit store data operand;

aligning said store data operand to said multiple bytes of data; and

updating said multiple bytes of data with said operand mask complement.

54. A method for a Load operation in a Load and Store operation unit comprising the steps of:

issuing an address generation instruction by a first instruction unit, said address generation instruction generating a real address in memory;

updating said real address in a real address field of a register in a Storage Reference Buffer;

sending concurrently, a request for a multiple byte word with said real address to said Storage Reference Buffer and a data cache;

receiving said multiple byte word from one of said Storage Reference Buffer and said data cache;

extracting selected bytes from said multiple byte word;

receiving said selected bytes by said first instruction unit; and

updating said multiple bytes of data with said operand mask complement.